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serializer or deserializer (LVDS SERDES) IP cores (ALTLVDS_TX and ALTLVDS_RX) implement the LVDS SERDES interfaces to transmit and receive high-speed differential data. You can configure the features of these IP cores using the IP Catalog and parameter editor.

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The Microtronix Video LVDS SerDes Transmitter / Receiver IP Core provides a complete, easy-to-use Serializer/Deserializer (SerDes) solution to interface a wide variety of video host systems to Flat Panel displays. The core simplifies the design of video LVDS interfaces, improves data integrity and timing margins.

~~Video LVDS SerDes Transmitter-Receiver IP Core~~

The Microtronix Video LVDS SerDes Transmitter / Receiver IP-Core. provides a complete, easy-to-use solution to interface with a wide variety of video host systems and flat panel displays. The core simplifies the design of video LVDS interfaces,

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improves data integrity and timing margins.

~~Microtronix Video LVDS SerDes Transmitter / Receiver IP Core~~

The LVDS_SERDES IP Core is a high-speed LVDS Transmitter/Receiver pair suitable for a wide range of serial interface applications. The design is comprised of an independent transmitter and receiver that may be used separately, or together as a single transceiver.

~~High-speed LVDS (SERDES) Transceiver Rev. 1~~

If you enable the Use External PLL option with the LVDS SERDES IP core transmitter and receiver, the following signals are required from the IOPLL Intel ® FPGA IP: Serial clock (fast clock) input to the SERDES of the

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LVDS SERDES IP core transmitter and receiver ; Load enable to the SERDES of the LVDS SERDES IP core transmitter and receiver

~~LVDS SERDES Intel FPGA IP User Guide: Intel Arria 10 and ...~~

All Stratix families support the Use Shared PLL(s) for Receiver and Transmitter option to place both the LVDS transmitter and the LVDS receiver in the same device I/O bank. The Quartus II software lets the transmitter and the receiver share the same fast PLL when both use the same input clock frequency.

~~SERDES Transmitter/Receiver (ALTLVDS) Megafunction User Guide~~
The SN65LVDS95 LVDS serdes (serializer/deserializer) transmitter contains three 7-bitparallel-loadserial-

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out shift registers, a 7 × clock synthesizer, and four low-voltage differential signaling (LVDS) line drivers in a single integrated circuit.

~~LVDS SERDES TRANSMITTER – TI.com~~

High-speed LVDS (SERDES) transceiver with up to 8 serial data lanes, generic data width and integrated asynchronous FIFO. Ideal for standard LVDS links such as Channel-link®, Camera-link®, FPD-link®, FlatLink®, MIPI etc. Capable of data rates of up to 500 Mbits/s per lane on basic FPGA devices and 1 Gbits/s+ on higher-end FPGAs.

~~High-Speed LVDS (SERDES) Transceiver IP Core~~

The synchronized LVDS data/parity and clock arrive at the receiver. The

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Receiver performs the conversion from LVDS to LVTTTL and the transceiver/parity generator performs the parity calculations. These devices compare their corresponding input bytes with the value received on the parity bit.

~~LVDS SERDES RECEIVER - TI.com~~

The SN65LVDS95 LVDS serdes (serializer/deserializer) transmitter contains three 7-bit parallel-load serial-out shift registers, a 7 × clock synthesizer, and four low-voltage differential signaling (LVDS) line drivers in a single integrated circuit.

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The Video LVDS SerDes Transmitter / Receiver IP Core simplifies the design

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of video LVDS interfaces, improves data integrity and timing margins. For example, the Transmitter has the ability to generate a LVDS transmit clock synchronous to the video data stream thereby eliminating the need to fine-tune a PLL to the outputted LVDS data.

~~Video LVDS SerDes Transmitter / Receiver IP Core~~

Low Voltage Differential Signaling, or LVDS, is an electrical signaling system that can run at very high speeds over cheap, twisted-pair copper cables. Applications: Firewire, SATA, SCSI. Differential Line Drivers and Receivers (LVDS PHY), Texas Instruments. LVDS Communication.

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