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Mashiko, K. Maegawa, S. and Inuishi, M.  
2001. Feasibility of 0.18  $\mu$ m SOI CMOS  
technology using hybrid trench isolation

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with high resistivity substrate for  
embedded RF/analog applications. IEEE

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## **The Design of CMOS Radio-Frequency Integrated Circuits**

Discover a fresh approach to efficient and  
insight-driven analog integrated circuit

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design in nanoscale-CMOS with this hands-on guide. Expert authors present a sizing methodology that employs ...

## **Systematic Design of Analog CMOS Circuits**

Design of CMOS digital integrated circuits, concentrating on device, circuit,

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and architectural issues. Analysis and design techniques in custom integrated circuit design, standard cells, memory. Use ...

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SICK unveiled the first in a new

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generation of Ruler3000 3D streaming cameras. The Ruler3000 line combines SICK's Ranger3 streaming camera with a Class 2 eye-safe laser, pre-selected optics and fixed ...

**SICK unveils new generation of  
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Mobix Labs Inc., a fabless RF (radio frequency) component company focused on next-generation wireless technologies, ...

**Mobix Labs Selected as Qualified  
Partner of the Japan External Trade  
Organization**

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Work aimed at extending the maximum frequency capability of CMOS technology, described in Chapters 5 and ... which provides a tunable linear resistive element for integrated circuit filter realisation ...

## **Chapter 8: Gallium Arsenide Analogue**

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## **Integrated Circuit Design Techniques**

Finishing up on the topic of CMOS bus logic I am going to show a ... Switching gears I am going to talk a bit about the physical layout of integrated circuits. Shown is an old wafer I have ...

## **How CMOS Works: Some Final Words**

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## **About CMOS**

A top-down guide to the design of digital integrated circuits. Reflects industry design methods, moving from VLSI architecture design to CMOS fabrication. Practical hints and tips, case studies, and

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**Digital Integrated Circuit Design from  
VLSI Architectures to CMOS  
Fabrication**

In this paper, a novel approach for very stable physical unclonable function (PUF) is presented based on randomly generated via-hole formation using standard CMOS ... integrated circuits. To guarantee ...

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## **VIA PUF: Ultimately Stable PUF Design using Random Via Formation in Standard CMOS Technology**

The Belgian research institute expects a prototype in standard 28-nm technology to be ready by the end of 2018. At the recent International Microwave Symposium in

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Philadelphia, Imec announced ...

## **Imec Demonstrates 140-GHz CMOS Radar-on-Chip with Integrated Antennas**

Wireless chipset / SoC design choices are driven by many orthogonal ... is moved to the RF chip and eventually enables an

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integrated single chip solution. The integration benefits of CMOS The key to

...

## **System on Chip (SoC) for Short Range Wireless - CMOS versus SiGe**

This structure also lets the company design membranes that are either flat or



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curved. The microphone chip measures 2.5 mm<sup>2</sup> and the diaphragm has a 1-mm diameter. The company says its CMOS MEMS ...

**Hear this: CMOS microphones on a chip**

of six-transistor SRAM-bit cells with an

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area less than 0.25 square microns—half the size of earlier solutions—using conventional bulk CMOS technology and 45nm design rules. Crolles 2 is the ...

**Alliance Produces Ultra-Dense SRAM Cell In 45nm CMOS Technology**  
reduce design space and complexity.

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Omivision also features advanced High Dynamic Range (HDR), which helps ensure high-quality image production in various lighting conditions for numerous ...

**3 New Image Signal Processors Target Power, Speed, and Autonomous Driving**

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Dual work function metal gates are integrated at 17nm spacing between n- and pFETs, highlighting the key benefit of forksheet devices for advanced CMOS area scaling ... Alternatively, with a forksheet ...

**Imec demoes integrated forksheet FETs**

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**for 2nm processes**

May 27, 2021 (Market Insight Reports) --  
“CMOS High-speed Cameras Market ...  
Mikrotron, Optronis, Integrated Design  
Tools, AOS Technologies, Fastec  
Imaging, Weisscam, Del Imaging Systems  
...

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**CMOS High-speed Cameras Market  
Size 2021 by Consumption, Volume,  
Average Price, Revenue, Market Share  
and Trend to 2028**

One technology used in the industry to mitigate this tradeoff is fully depleted silicon-on-insulator (FD-SOI) technology which can operate at 75% lower power as

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compared to a bulk CMOS process ... “We  
...

## **Lattice Leverages FD-SOI for New Low Power FPGAs**

With our third generation Keystone DSP design, and the power advantages of 5nm CMOS technology, we are directly

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addressing our customers' critical needs  
for low power, highly integrated, high ...

## **MaxLinear Showcases Industry's First 5nm CMOS 800G PAM4 DSP on TSMC Advanced Process at OFC 2021**

Intevac, Inc. (Nasdaq: IVAC) announced  
today that it has received two additional



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Phase 1 development program awards in  
Photonics. These awards are ...

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